REMARKS/ARGUMENTS

Pending claims 16 and 18 stand rejected under 35 U.S.C. § 102(e) over U.S. Patent Publication No. 2002/0128037 (Schmidt). Applicant respectfully traverses the rejection. As to claim 16, the Office Action contends that Schmidt teaches switching a system to process an instruction of a second processor family instruction set in a second core portion of a reconfigurable processor core (that includes a first core portion configured to process instructions belonging to a first processor family instruction set). Applicant respectfully disagrees for several reasons. First, Schmidt nowhere teaches switching a system to process such second family instructions. Instead, all that Schmidt teaches in the indicated passage is that a reconfigurable core includes decoders and a multiplexer. Schmidt, ¶16-17. While this may be so, Schmidt fails to teach or suggest that these structures switch a system to process instructions of a second processor family instruction set in a second core portion of the reconfigurable processor core. Instead, presumably the reconfigurable processor core of Schmidt is all of a single processor family instruction set, as there is no teaching of different core portions to process instructions belonging to different family instruction sets. Still further, there is no second switching step disclosed in Schmidt. That is, Schmidt further fails to teach switching the system to process a second instruction of the first processor family instruction set after processing the instruction of the second processor family instruction set. Accordingly, the anticipation rejection of claims 16 and 18 is overcome.

Pending claims 1, 4-15 and 19 stand rejected under 35 U.S.C. § 103(a) over Schmidt in view of U.S. Patent No. 5,490,101 (Lee). Applicant respectfully traverses the rejection. As to claim 1, the Office Action contends that Schmidt teaches the recited reconfigurable processor core that includes both a first core portion configured to process instructions belonging to a first host processor family and a second core portion configured to process instructions belonging to a second host processor family. As contended support, the Office Action points to the indication that processors 151 of the reconfigurable processor core can be MIPS (i.e., RISC) processors. Furthermore, while the Office Action notes that the reconfigurable processor core of Schmidt can further include DSPs and ASICs, there is no teaching or suggestion in Schmidt that these components be of a second host processor family. Presumably instead, they are of the same host processor family as the remainder of the reconfigurable processor core of Schmidt, as there is nothing in the reference to indicate otherwise.

Furthermore, as described above regarding claim 16, Schmidt fails to teach or suggest the recited processor type select circuit since nothing in the instruction decoders and multiplexer of Schmidt is taught to be used to configure an integrated circuit to process instructions belonging to instruction sets of one of two different host processor families.

The rejection is further respectfully traversed as there is no reason one of ordinary skill in the art would combine the teaching of Schmidt with that of Lee. Instead, Lee merely teaches a data multiplying circuit. Simply put, nothing in Lee anywhere suggests the combination of its digital data multiplying circuit with the reconfigurable processor core of Schmidt. Instead, all the Office Action points to in Lee is the Field of Invention, which states the conventional implementation of a DSP that includes multiple digital data processing functions in a single chip. Lee, col. 1, lns. 21-27. This nowhere teaches or suggests the integration of a host processor, reconfigurable processor core, and processor type select circuit in a single integrated circuit.

For at least the same reasons as described above regarding claim 1, its dependent claims as well as dependent claim 19 also are patentable in view of the cited art.

The application is believed to be in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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